

ABSTRACT

Systems, methodologies, media, and other embodiments associated with reducing a bounding box for a net in a VLSI design of cells, where a cell may have two or more pins by which it can be connected to one or more other cells in the design, is described. One
5 exemplary method may include receiving the design, producing an initial bounding box for a net in the design, and reducing the initial bounding box to a reduced bounding box.